MALLA REDDY ENGINEERING COLLEGE

(Autonomous)

Maisammaguda, Dhulapally,Secunderabad – 500100

II B.Tech I Semester, CSE(AIML)

Mid Term Examinations-II

Subject Code & Name: - **C0509 & Computer Organization and Architecture**

Marks: **25M** Time: **90 Mins**

Answer ALL the Questions Date:

S.No.	Questions	Marks	BT Level	CO
	Module-3			
1	Evaluate multiplication of two numbers using Multiplication algorithm with a numerical example.	5	2	3
2	Write an algorithm to add the magnitudes and attach the sign of A to the result, when the signs of A and B are different.	5	2	3
3	Use the flow chart for division algorithm and solve AQ=0111000000 divided by B=10001	5	2	3
4	Using flowchart discuss the hardware algorithm for subtraction.	5	2	3

S.No.	Questions	Marks	BT Level	CO
	Module-4			
1	Analyze the 3 different mapping processes used in cache memory organization.	5	2	4
2	Explain Daisy Chaining and Parallel Priority Interrupt with the help of a neat sketch	5	2	4
3	Interpret the Memory Connection to CPU by using Memory Address Mapping of RAM Chip and ROM Chip	5	3	4
4	Explain a) Auxiliary Memory b) Associate Memory	5	2	4
5	Sketch the block diagram of DMA using DMA Controller	5	2	4
6	Explain the different types of modes of transfer in detail	5	3	4
7	Describe the asynchronous data transfer	5	2	4
8	Explain memory hierarchy in memory organization	5	2	4

S.No.	Questions	Marks	BT Level	CO
	Module-5			
1	Write a brief note on interprocessor arbitration	5	2	5
2	Difference between RISC and CISC	5	2	5
3	Write about Interprocessor communication and Synchronization	5	2	5
4	List out the important stages of Instruction Pipeline	5	2	5
5	Illustrate about Flynn's Classification of parallel processing.	5	2	5
6	What is parallel processing? Explain any parallel processing mechanism	5	2	5
7	Explain the interconnection structure for multiprocessor systems	5	2	5
8	What is multiprocessor system? Explain the advantages of multi processors over uniprocessors.	5	2	5

Course Instructor Name: Dr. U. Mohan Srinivas

Signature: **HOD Signature**

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OBJECTIVE QUESTION BANK

Answer ALL the Questions

		ANS
1	The fastest data access is provided using _____.	D
	a) Caches	
	b) DRAM's	
	c) SRAM's	
	d) Registers	
2	The effectiveness of the cache memory is based on the property of _____	A
	a) Locality of reference	
	b) Memory localization	
	c) Memory size	
	d) None of the above	
3	The correspondence between the main memory blocks and those in the cache is given by _____.	C
	a) Hash function	
	b) Locale function	
	c) Mapping function	
	d) Assign function	
4	The algorithm to remove and place new contents into the cache is called __	A
	a) Replacement algorithm	
	b) Updation	
	c) Renewal algorithm	
	d) None of the above	
5	The bit used to signify that the cache location is updated is _____.	A
	a) Dirty bit	
	b) Update bit	
	c) Reference bit	
	d) Flag bit	
6	The last on the hierarchy scale of memory devices is _____.	B
	a) Main memory	
	b) Secondary memory	
	c) TLB	
	d) Flash drives	
7	In memory interleaving, the lower order bits of the address is used to	C
	a) Get the data	
	b) Get the address of the data within the module	
	c) Get the address of the module	
	d) None of the above	
8	The number of successful accesses to memory stated as a fraction is called as _____.	A
	a) Hit rate	
	b) Miss rate	
	c) Success rate	
	d) Access rate	

9	The number of failed attempts to access memory, stated in the form of fraction is called as _____.	B
	a) Hit rate	
	b) Miss rate	
	c) Failure rate	
	d) Delay rate	
10	In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one, when _____ occurs.	B
	a) Delay	
	b) Miss	
	c) Hit	
	d) Delayed hit	
11	The extra time needed to bring the data into memory in case of a miss is called as _____.	C
	a) Delay	
	b) Propagation time	
	c) Miss penalty	
	d) None of the above	
12	The key factor/s in commercial success of a computer is/are _____.	D
	a) Performance	
	b) Cost	
	c) Speed	
	d) Both a and b	
13	The main objective of the computer system is	B
	a) To provide optimal power operation.	
	b) To provide best performance at low cost.	
	c) To provide speedy operation at low power consumption.	
	d) All of the above.	
14	The main purpose of having memory hierarchy is to	D
	a) Reduce access time.	
	b) Provide large capacity.	
	c) Reduce propagation time.	
	d) Both a and b.	
15	The program is divided into operable parts called as _____.	B
	a) Frames	
	b) Segments	
	c) Pages	
	d) Sheets	
16	The techniques which move the program blocks to or from the physical memory is called as _____.	B
	a) Paging	
	b) Virtual memory organization	
	c) Overlays	
	d) Framing	
17	The binary address issued to data or instructions are called as _____.	D
	a) Physical address	
	b) Location	
	c) Relocatable address	
	d) Logical address	
18	_____is used to implement virtual memory organization.	C
	a) Page table	
	b) Frame table	
	c) MMU	
	d) None of the above	
19	_____ translates logical address into physical address.	A

	a) MMU	
	b) Translator	
	c) Compiler	
	d) Linker	
20	The main aim of virtual memory organization is	D
	a) To provide effective memory access.	
	b) To provide better memory transfer.	
	c) To improve the execution of the program.	
	d) All of the above.	
21	The virtual memory basically stores the next segment of data to be executed on the _____.	A
	a) Secondary storage	
	b) Disks	
	c) RAM	
	d) ROM	
22	For the synchronization of the read head, we make use of a _____.	C
	a) Framing bit	
	b) Synchronization bit	
	c) Clock	
	d) Dirty bit	
23	Floating-point numbers are normally a multiples of size of	C
	a) Bit	
	b) Nibble	
	c) Word	
	d) Byte	
24	A 4 digit BCD number can be represented with the help of	B
	a) 10 bits	
	b) 16 bits	
	c) 8 bits	
	d) 12 bits	
25	Any electronic holding place where data can be stored and retrieved later whenever required is _____	A
	a) Memory	
	b) Drive	
	c) Disk	
	d) Circuit	
26	The logic operations are implemented using _____ circuits.	C
	a) Bridge	
	b) Logical	
	c) Combinational	
	d) Gate	
27	The carry generation function: ci + 1 = yici + xici + xiyi, is implemented in	B
	a) Half adders	
	b) Full adders	
	c) Ripple adders	
	d) Fast adders	
28	The carry in the ripple adders, (which is true)	C
	a) Are generated at the beginning only.	
	b) Is generated at the end of each operation.	
	c) Must travel through the configuration.	
	d) None of the above	
29	In full adders the sum circuit is implemented using _____ gates.	C
	a) AND & OR	
	b) NAND	
	c) XOR	

	d) XNOR	
30	The usual implementation of the carry circuit involves _____ gates.	B
	a) AND & OR	
	b) XOR	
	c) NAND	
	d) XNOR	
31	A _____ gate is used to detect the occurrence of an overflow.	B
	a) NAND	
	b) XOR	
	c) XNOR	
	d) AND	
32	In a normal adder circuit the delay obtained in generation of the output is	A
	a) 2n + 2	
	b) 2n	
	c) n + 2	
	d) None of the above	
33	The final addition sum of the numbers, 0110 & 0110 is	A
	a) 1101	
	b) 1111	
	c) 1001	
	d) 1010	
34	The delay reduced to in the carry look ahead adder is _____.	A
	a) 5	
	b) 8	
	c) 10	
	d) 2n	
35	We make use of _____ circuits to implement multiplication.	C
	a) Flip flops	
	b) Combinatorial	
	c) Fast adders	
	d) None of the above	
36	The multiplier is stored in _____.	B
	a) PC Register	
	b) Shift register	
	c) Cache	
	d) None of the above	
37	The _____ is used to co-ordinate the operation of the multiplier.	C
	a) Controller	
	b) Coordinator	
	c) Control sequencer	
	d) None of the above	
38	The multiplicand and the control signals are passed through to the n-bit adder via _____.	A
	a) MUX	
	b) DEMUX	
	c) Encoder	
	d) Decoder	
39	The method used to reduce the maximum number of summands by half is ____.	B
	a) Fast multiplication	
	b) Bit-pair recording	
	c) Quick multiplication	
	d) None of the above	
40	CSA stands for	A
	a) Computer Speed Addition	
	b) Computer Service Architecture	

	c) Carry Save Addition	
	d) None of the above	
41	The numbers written to the power of 10 in the representation of decimal numbers are called as _____.	C
	a) Height factors	
	b) Size factors	
	c) Scale factors	
	d) None of the above	
42	If the decimal point is placed to the right of the first significant digit, then the number is called as _____.	B
	a) Orthogonal	
	b) Normalized	
	c) Determinate	
	d) None of the above	
43	_____ constitute the representation of the floating number.	D
	a) Sign	
	b) Significant digits	
	c) Scale factor	
	d) All of the above	
44	The sign followed by the string of digits is called as _____.	C
	a) Significant	
	b) Determinant	
	c) Mantissa	
	d) Exponent	
45	In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.	B
	a) 24	
	b) 23	
	c) 20	
	d) 16	
46	The 32 bit representation of the decimal number is called as ____.	B
	a) Double-precision	
	b) Single-precision	
	c) Extended format	
	d) None of the above	
47	In 32 bit representation the scale factor is a range of _____.	A
	a) -128 to 127	
	b) -256 to 255	
	c) 0 to 255	
	d) None of the above	
48	When the processor executes multiple instructions at a time it is said to use ___	D
	a) Single issue	
	b) Multiplicity	
	c) Visualization	
	d) Multiple issue	
49	The _____ plays a very vital role in case of super scalar processors.	A
	a) Compilers	
	b) Motherboard	
	c) Memory	
	d) Peripherals	
50	In super-scalar processors, _____ mode of execution is used.	C
	a) In-order	
	b) Post order	
	c) Out of order	
	d) None of the mentioned	

51	In memory-mapped I/O…	A
	a) The I/O devices and the memory share the same address space	
	b) The I/O devices have a separate address space	
	c) The memory and I/O devices have an associated address space	
	d) A part of the memory is specifically set aside for the I/O operation	
52	The usual BUS structure used to connect the I/O devices is	B
	a) Star BUS structure	
	b) Single BUS structure	
	c) Multiple BUS structure	
	d) Node to Node BUS structure	
53	The advantage of I/O mapped devices to memory mapped is	C
	a) The former offers faster transfer of data	
	b) The devices connected using I/O mapping have a bigger buffer space	
	c) The devices have to deal with fewer address lines	
	d) No advantage as such	
54	To overcome the lag in the operating speeds of the I/O device and the processor we use	B
	a) Buffer spaces	
	b) Status flags	
	c) Interrupt signals	
	d) Exceptions	
55	The method of accessing the I/O devices by repeatedly checking the status flags is	A
	a) Program-controlled I/O	
	b) I/O mapped	
	c) Memory-mapped I/O	
	d) None	
56	The method which offers higher speeds of I/O transfers is	D
	a) Interrupts	
	b) Memory mapping	
	c) Program-controlled I/O	
	d) DMA	
57	The process where in the processor constantly checks the status flags is called as	A
	a) Polling	
	b) Inspection	
	c) Reviewing	
	d) Echoing	
58	As the instructions can deal with variable size operands we use _____ to resolve this	B
	a) Delimiter	
	b) Size indicator mnemonic	
	c) Special assemblers	
	d) None of the above	
59	The starting address is denoted using _____ directive	C
	a) EQU	
	b) ORIGIN	
	c) ORG	
	d) PLACE	
60	The constant can be declared using ____ directive	D
	a) DATAWORD	
	b) PLACE	
	c) CONS	
	d) DC	
61	To allocate a block of memory we use ____ directive	B
	a) RESERVE	
	b) DS	
	c) DATAWORD	

	d) PLACE	
62	The Branch instruction in 68000 provides how many types of offsets?	D
	a) 3	
	b) 1	
	c) 0	
	d) 2	
63	The DMA transfers are performed by a control circuit called as	B
	a) Device interface	
	b) DMA controller	
	c) Data controller	
	d) Overlooker	
64	In DMA transfers, the required signals and addresses are given by the	C
	a) Processor	
	b) Device drivers	
	c) DMA controllers	
	d) The program itself	
65	The DMA controller has _____ registers	C
	a) 4	
	b) 2	
	c) 3	
	d) 1	
66	The controller is connected to the ____	B
	a) Processor BUS	
	b) System BUS	
	c) External BUS	
	d) None of the above	
67	The technique where the controller is given complete access to main memory is	D
	a) Cycle stealing	
	b) Memory stealing	
	c) Memory Con	
	d) Burst mode	
68	To overcome the conflict over the possession of the BUS we use _____	B
	a) Optimizers	
	b) BUS arbitrators	
	c) Multiple BUS structure	
	d) None of the above	
69	The registers of the controller are _____	C
	a) 64 bits	
	b) 24 bits	
	c) 32 bits	
	d) 16 bits	
70	The DMA transfer is initiated by _____	C
	a) Processor	
	b) The process being executed	
	c) I/O devices	
	d) OS	
71	_____ interrupt method uses register whose bits are set separately by interrupt signal for each device	A
	a) Parallel priority interrupt	
	b) Daisy chaining	
	c) Serial priority interrupt	
	d) None of the above	
72	____ register is used for the purpose of controlling the status of each interrupt request in parallel priority interrupt	D
	a) Mass	

	b) Mark	
	c) Make	
	d) Mask	
73	Interrupts initiated by an instruction is called as	B
	a) Internal	
	b) External	
	c) Hardware	
	d) Software	
74	The signals that are provided to maintain proper data flow and synchronization between the data transmitter and receiver are	A
	a) Handshaking signals	
	b) Control signals	
	c) Input signals	
	d) None of the above	
75	The example of output device is	D
	a) CRT display	
	b) 7-segment display	
	c) Printer	
	d) All of the mentioned	
76	_____ have been developed specifically for pipelined systems.	C
	a) Utility software	
	b) Speed up utilities	
	c) Optimizing compilers	
	d) None of the mentioned	
77	The pipelining process is also called as _____.	B
	a) Superscalar operation	
	b) Assembly line operation	
	c) Von Neumann cycle	
	d) None of the mentioned	
78	The fetch and execution cycles are interleaved with the help of _____.	C
	a) Modification in processor architecture	
	b) Special unit	
	c) Clock	
	d) Control unit	
79	Each stage in pipelining should be completed within ____ cycle.	A
	a) 1	
	b) 2	
	c) 3	
	d) 4	
80	Size of the _____ memory mainly depends on the size of the address bus.	A
	a) Main	
	b) Virtual	
	c) Secondary	
	d) Cache	
81	If a unit completes its task before the allotted time period, then	C
	a) It'll perform some other task in the remaining time	
	b) Its time gets reallocated to different task	
	c) It'll remain idle for the remaining time	
	d) None of the mentioned	
82	To increase the speed of memory access in pipelining, we make use of	C
	a) Special memory locations	
	b) Special purpose registers	
	c) Cache	
	d) Buffers	
83	Which of the following is independent of the address bus?	A

	a) Secondary memory	
	b) Main memory	
	c) Onboard memory	
	d) Cache memory	
84	The iconic feature of the RISC machine among the following is _____	C
	a) Reduced number of addressing modes	
	b) Increased memory size	
	c) Having a branch delay slot	
	d) All of the mentioned	
85	Both the CISC and RISC architectures have been developed to reduce the _____	C
	a) Cost	
	b) Time delay	
	c) Semantic gap	
	d) All of the mentioned	
86	Which control refers to the track of the address of instructions	C
	a) Data control	
	b) Register control	
	c) Program control	
	d) None of these	
87	In program control the instruction is set for the statement in:	B
	a) Parallel	
	b) Sequence	
	c) Both	
	d) None	
88	SIMD stands for:	D
	a) System instruction multiple data	
	b) Scale instruction multiple data	
	c) Symmetric instruction multiple data	
	d) Single instruction multiple data	
89	MIMD stands for:	C
	a) Multiple input multiple data	
	b) Memory input multiple data	
	c) Multiple instruction multiple data	
	d) Memory instruction multiple data	
90	Which is a method of decomposing a sequential process into sub operations?	A
	a) Pipeline	
	b) CISC	
	c) RISC	
	d) Database	
91	Which are the types of array processor?	C
	a) Attached array processor	
	b) SIMD array processor	
	c) Both	
	d) None	
92	Which type of register holds a single vector containing at least two read ports and one write ports	D
	a) Data system	
	b) Database	
	c) Memory	
	d) Vector register	
93	Which is used to speed-up the processing:	C
	a) Pipeline	
	b) Vector processing	
	c) Both	
	d) None	

94	Which processor is a peripheral device attached to a computer so that the performance of a computer can be improved for numerical computations?	A
	a) Attached array processor	
	b) SIMD array processor	
	c) Both	
	d) None	
95	Which processor has a single instruction multiple data stream organization that manipulates the common instruction by means of multiple functional units?	B
	a) Attached array processor	
	b) SIMD array processor	
	c) Both	
	d) None	
96	Processor without structural hazard is	A
	a) Faster	
	b) Slower	
	c) Have longer clock cycle	
	d) Have larger clock rate	
97	Simplest scheme to handle branches is to	D
	a) Flush pipeline	
	b) Freezing pipeline	
	c) Depth of pipeline	
	d) Both a and b	
98	Splitting cache into separate instructions and data caches or by using a set of buffers, usually called	C
	a) Cache buffer	
	b) Data buffer	
	c) Instruction buffer	
	d) None of above	
99	With separate adder and a branch decision made during ID, there is only a	A
	a) 1-clock-cycle stall on branches	
	b) 2-clock-cycles stall on branches	
	c) 4-clock-cycles stall on branches	
	d) 3-clock-cycles stall on branches	
100	Load instruction has a delay or latency that cannot be eliminated by forwarding, other technique used is	A
	a) Pipeline interlock	
	b) Deadlock	
	c) Stall interlock	
	d) Stall deadlock	
101	If event occurs at same place every time program is executed with same data and memory allocation, then event is known as	B
	a) Stalled	
	b) Synchronous	
	c) Delayed	
	d) Asynchronous	
102	Pipeline overhead arises from combination of pipeline register delay and	D
	a) Hit rate	
	b) Clock cycle	
	c) Cycle rate	
	d) Clock skew	
103	Each of clock cycles from previous section of execution, becomes a	A
	a) Pipe stage	
	b) Previous stage	
	c) Stall	
	d) Processor cycle	

104	Exceptions that occur within instructions are usually	A
	a) Synchronous	
	b) Asynchronous	
	c) Pipelined	
	d) Blocked	
105	When compiler attempts to schedule instructions to avoid hazard; this approach is called	D
	a) Compiler	
	b) Static scheduling	
	c) Dynamic scheduling	
	d) Both a and b	
106	Pipelining increases CPU instruction	B
	a) Size	
	b) Through put	
	c) Cycle rate	
	d) Time	
107	Sum of contents of base register and sign-extended offset is used as a memory address, sum is known as	C
	a) ALU instructions	
	b) Through put	
	c) Effective address	
	d) Load and store instructions	
108	Process of letting an instruction move from instruction decode stage into execution stage of this pipeline is usually called	B
	a) Canceling	
	b) Instruction issue	
	c) Nullifying	
	d) Branch prediction	
109	If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _____	B
	a) Exception handling	
	b) Imprecise exceptions	
	c) Error correction	
	d) None of the mentioned	
110	The product of 1101 & 1011 is _____	A
	a) 10001111	
	b) 10101010	
	c) 11110000	
	d) 11001100	
111	Code containing redundant loads, stores, and other operations that might be eliminated by an optimizer, is	D
	a) Optimized clock	
	b) Unoptimized clock	
	c) Optimized code	
	d) Unoptimized code	
112	Delays arising from use of a load result 1 or 2 cycles after loads, refers as	D
	a) Data stall	
	b) Control stall	
	c) Branch stall	
	d) Load stall	
113	Situations that prevent next instruction in instruction stream, from executing during its designated clock cycle are known	C
	a) Pipe stage	
	b) Previous stage	
	c) Hazards	
	d) Processor cycle	

114	The product of -13 & 11 is	B
	a) 1100110011	
	b) 1101110001	
	c) 1010101010	
	d) 1111111000	
115	The method used to reduce the maximum number of summands by half is _____	B
	a) Fast multiplication	
	b) Bit-pair recording	
	c) Quick multiplication	
	d) None of the mentioned	
116	The digital information is stored on the hard disk by _____	A
	a) Applying a suitable electric pulse	
	b) Applying a suitable magnetic field	
	c) Applying a suitable nuclear field	
	d) By using optic waves	
117	A hard disk with 20 surfaces will have _____ heads.	D
	a) 10	
	b) 5	
	c) 1	
	d) 20	
118	The read and write operations usually start at _____ of the sector.	D
	a) Center	
	b) Middle	
	c) From the last used point	
	d) Boundaries	
119	The associatively mapped virtual memory makes use of _____	A
	a) TLB	
	b) Page table	
	c) Frame table	
	d) None of the mentioned	
120	If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is a term of the Basic performance equation)	C
	a) 3	
	b) ~2	
	c) ~1	
	d) 6	
121	Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?	A
	a) A	
	b) B	
	c) Both take the same time	
	d) Insufficient information	
122	An effective to introduce parallelism in memory access is by _____	A
	a) Memory interleaving	
	b) TLB	
	c) Pages	
	d) Frames	
123	The performance depends on _____	B
	a) The speed of execution only	
	b) The speed of fetch and execution	
	c) The speed of fetch only	
	d) The hardware of the system only	
124	A common measure of performance is _____	A

	a) Price/performance ratio	
	b) Performance/price ratio	
	c) Operation/price ratio	
	d) None of the above	
125	The bits 1 & 1 are recorded as _____ in bit-pair recording.	D
	a) -1	
	b) 0	
	c) +1	
	d) Both -1 and 0	

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